SERVICE MANUAL & PARTS LIST (with price)

SF-5600AR(LX-589)

MAR. 1994

SF-5600AR

INDEX

CASIO®

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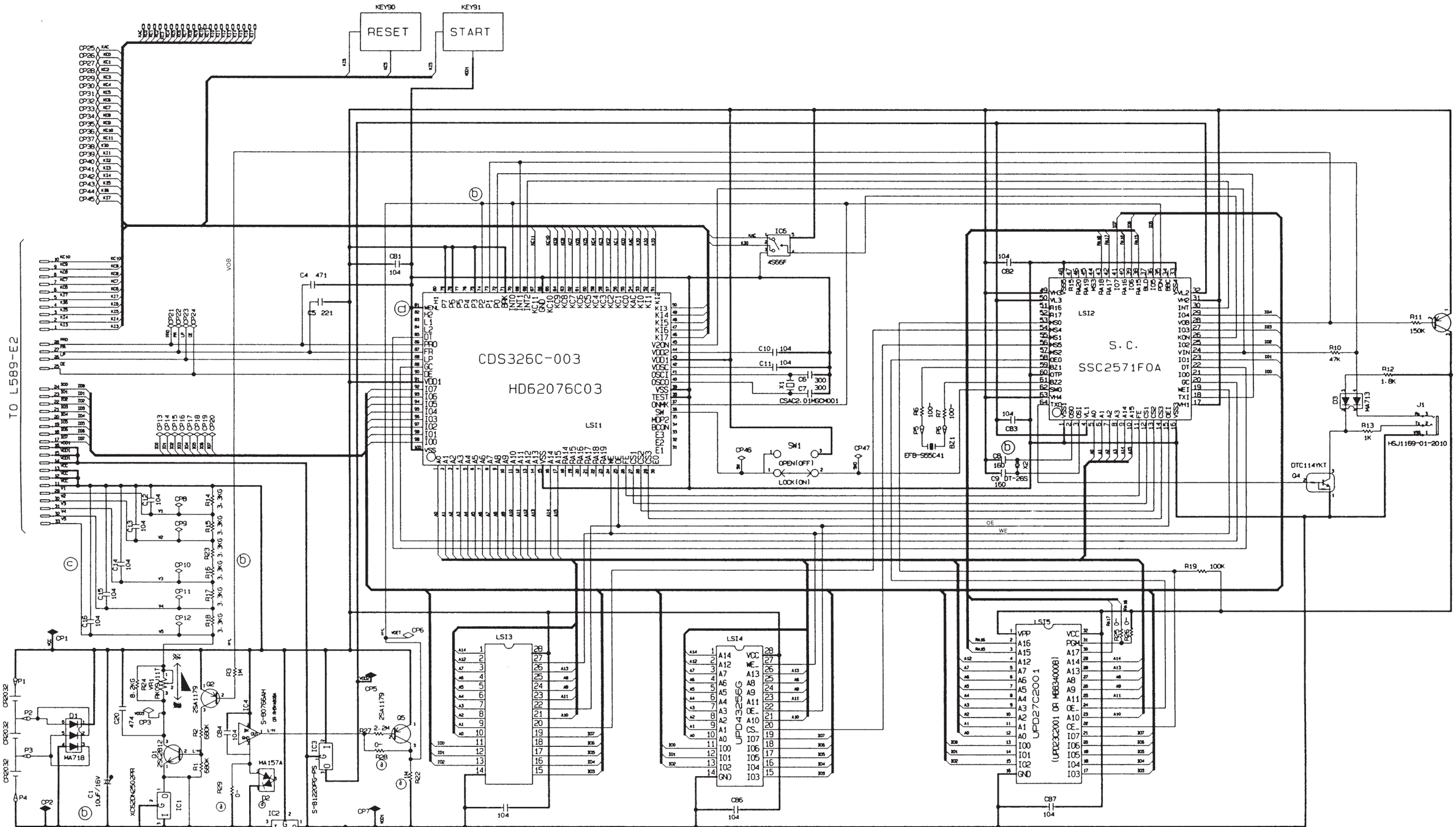
1. SCHEMATIC DIAGRAM

1-1. Main PCB

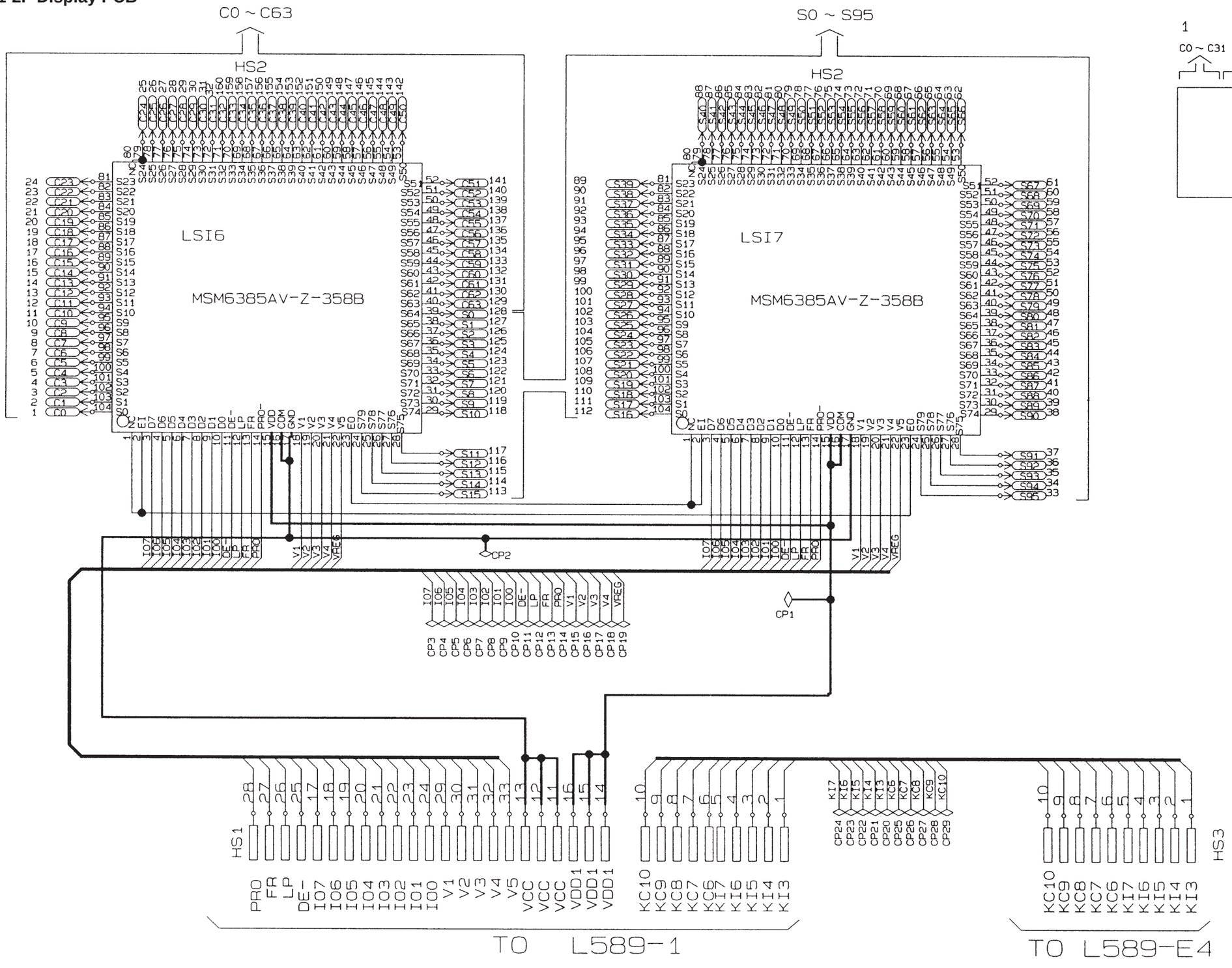


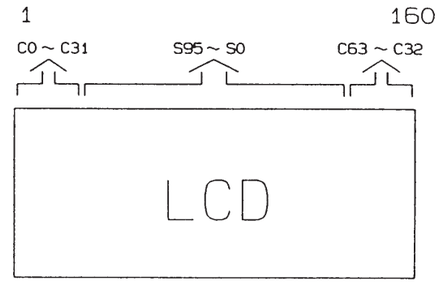
IC4	D2	Q5	R22	R27	R28	R29
S-80766AH	—	○	○	○	—	○
RH5VA50BA	○	—	○	—	○	—

NOTE: 1. The following parts are not used.
C2, C3, C17~C19, IC1, R4, R5, R8, R9, R20, R21, R24, R25, R27

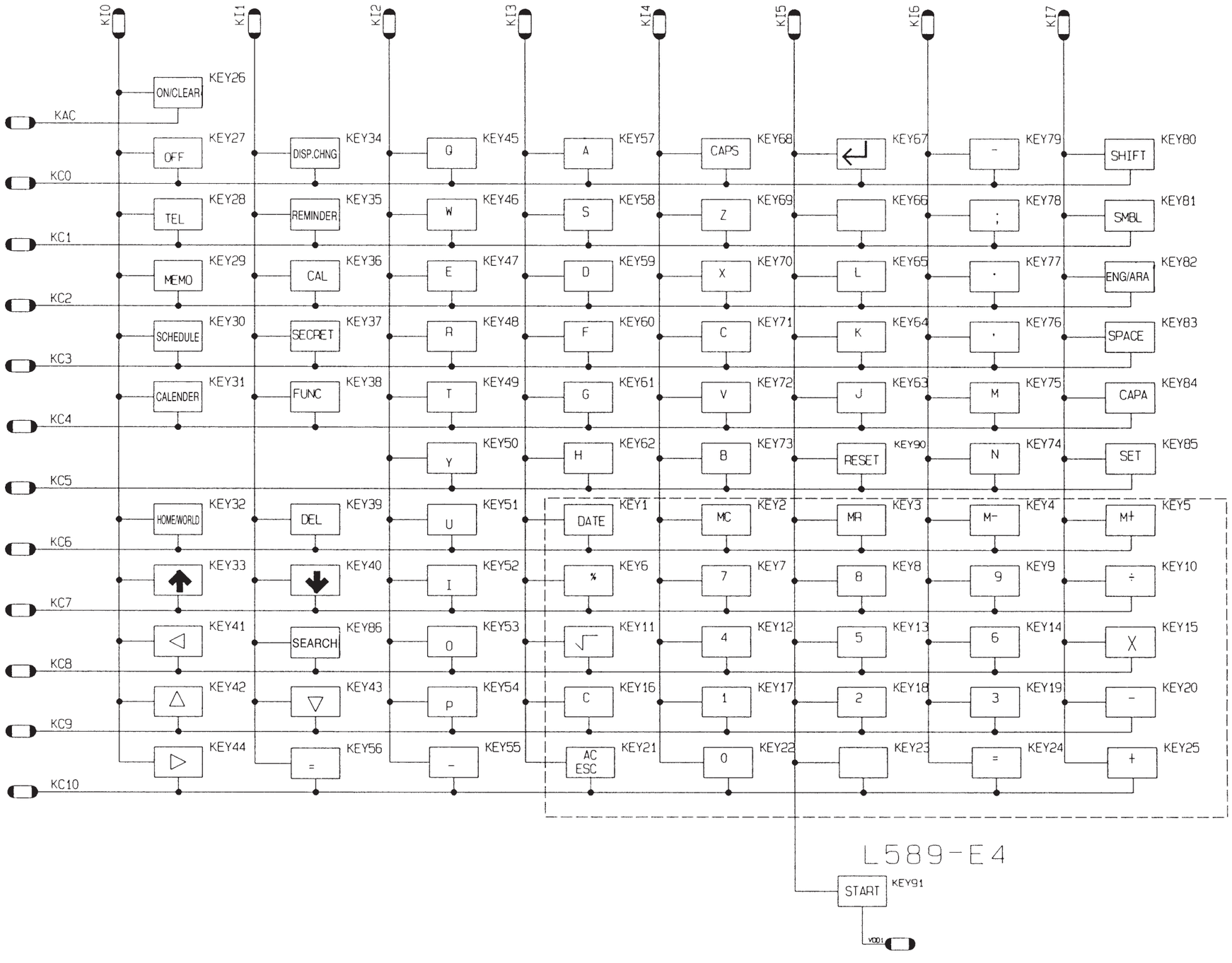
2. The following parts are not assembled.
CB5, LSI3.

1-2. Display PCB

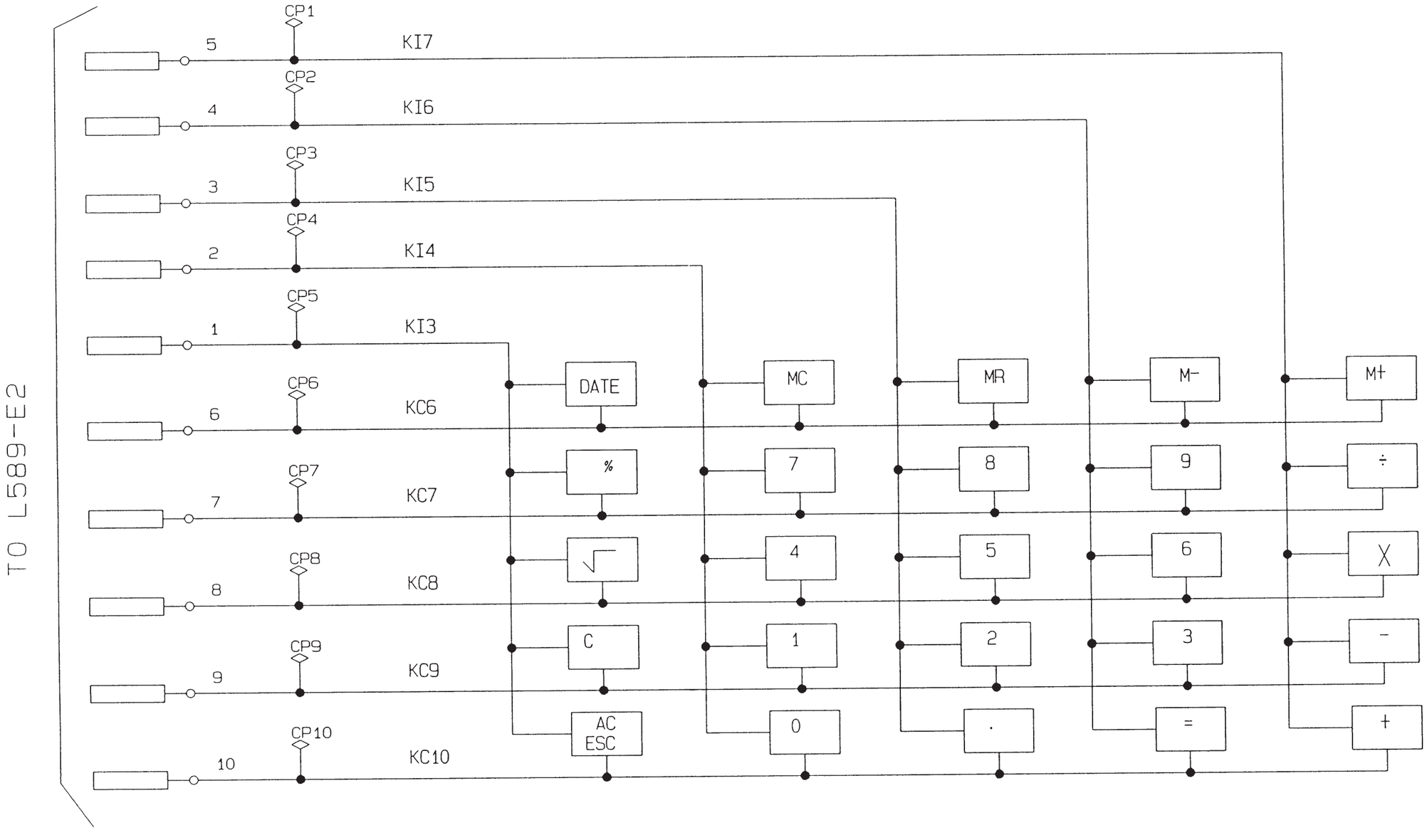




1-3. Key Matrix



1-4. Key Matrix (Display side)



2. SPECIFICATIONS

Main modes: Telephone Directory, Memo, Schedule Keeper, Reminder, Calendar (Gregorian and Hijira formats), Calculator

Clock: Home Time and World Time
Accuracy under normal temperatures: ±3 seconds a month

Alarm functions: Daily Alarm, Schedule Alarm and Reminder Alarm

Calculation: 12-digit arithmetic calculations; arithemetic constants (+, –, x, ÷); independent memory; percentages; square roots; 24-digit approximations; date calculations; other mixed calculations

Display element: LCD; 16-column × 8-line (Alpha Input Mode) /
12-column × 4-line (Arabic Input Mode)
Memory capacity: 32KB (24443 bytes)
Main component: LSI
Power supply: 3 lithium batteries (CR2032)
Power consumption: 0.07W
Battery life: Approximately 180 hours continuous operation in Telephone Directory; approximately 140 hours repeating one minute of input and 10 minutes of display in Telephone Directory; approximately 18 months for memory back up
Auto power off: Approximately 6 minutes after last key operation
Operating temperature: 0°C ~ 40°C (32°F ~ 104°F)
Dimensions:
Unfolded: 9.55(H) × 144(W) × 155(D)mm
Folded: 15.95(H) × 144(W) × 77.5(D)mm
Weight: 123g

• Design and specifications are subject to change without notice.

Current consumption:

Power switch	TYP. [μA]	MAX [μA]
OFF	11.7	37.1
ON	870	9,745
ON (Operating)	5,330	14,645

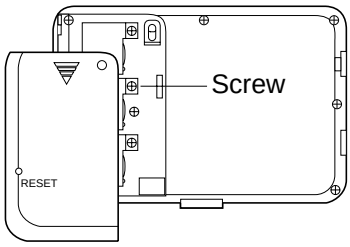
3. TO REPLACE THE BATTERY

To replace the batteries

1. Loosen the screw on the back of the SF Unit that holds the battery compartment cover in place, and remove the cover.

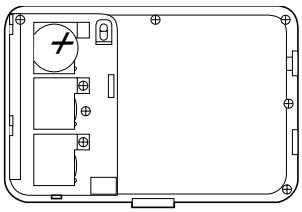
Caution

In the next step, be sure to remove only one battery at a time. Otherwise, you will lose all data stored in memory.



2. Loosen the screw that secures one of the three battery holders in place and remove the battery holder.

3. Replace the old battery with a new one, making sure that the positive (+) side of the new battery is facing up (so you can see it).



4. Replace the battery holder and secure it by tightening its screw.

- Be careful that you do not over tighten the screw.

5. Repeat steps 2 through 4 for the other two batteries.

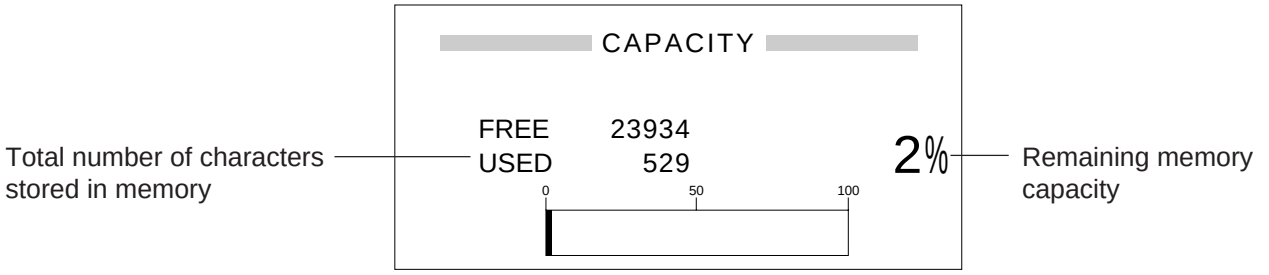
- Be sure to replace all three batteries. Never mix old batteries with new ones, and be sure to use CR2032 lithium batteries only.

6. After you replace all three batteries, replace the battery compartment cover and secure it by tightening its screw.

- Be careful that you do not over tighten the screw.

4. TO CHECK THE MEMORY CAPACITY

Hold down CAPA to display a screen that shows the current memory status. To clear the memory status display, release CAPA .



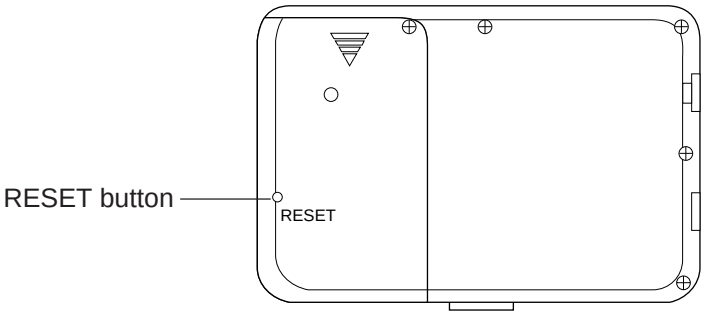
5. ERROR MESSAGE

Message	Meaning	Action
NO DATA!	Search operation attempted when no data is stored in memory.	Current search operation cannot be performed.
NOT FOUND!	Data specified in search operation does not exist in memory.	Change specification or cancel search.
MEMORY FULL!	No more room in memory for storage of data.	Delete unnecessary data items from memory.
ALARM TIME ALREADY USED!	Attempt to set a Schedule Keeper alarm time that is already used for another entry.	Set a different alarm time or change the existing alarm time to another one.
ALARM TIME ALREADY PASSED!	Attempt to set a Schedule Keeper alarm time for a time/date that is already passed.	Set a different alarm time (for a future time/date.)
SECRET DATA!	Alarm for a secret memory area data item is sounding.	Enter the secret memory area to view details of the alarm.
PASSWORD MISMATCH!	Attempt to enter the secret memory area using a password that does not match the one preset for the secret area.	Use the correct password.
TRANSMIT ERROR! STOPPED!	Error during data communications.	Cancel the data communications operation and try again.
DATA ERROR! CONSULT THE OWNER'S MANUAL!	Data corrupted by strong impact, electrostatic charge, etc.	See page 9 of owner's manual.

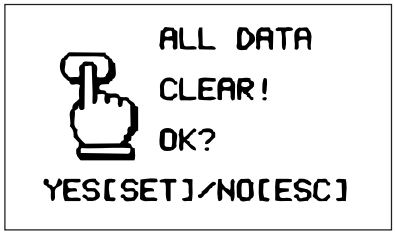
6. TO RESET THE DIGITAL DIARY

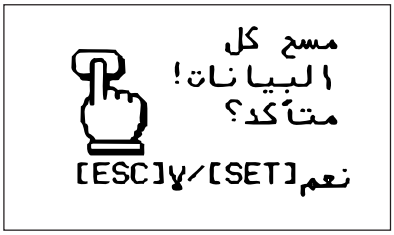
The following procedure erases all data stored in the memory of the SF Unit, including mark protected data. Perform the following operation only when you want to delete all data and initialize the settings of the SF Unit.
Remember — you should always keep copies of important data by writing it down, by transferring it to a personal computer or other SF Unit.

To reset the SF Unit's memory



1. Press the **RESET** button.





Important!
The next step deletes all data stored in the SF Unit's memory. Make sure that you really want to delete the data before you continue!

2. Press SET to reset the memory and delete all data or ESC to abort the reset operation without deleting anything.

Following the reset operation described above, the Home Time display appears and the SF Unit settings are initialized as noted below.

Home Time:	G. M. T. 1995/1/1 SUN 12:00 AM 12-hour format
World Time:	Tokyo
Daily Alarm:	12:00 PM
Sound:	Schedule alarm — ON Reminder alarm — ON Daily alarm — OFF Key — ON
Message:	Arabic
Character input:	CAPS

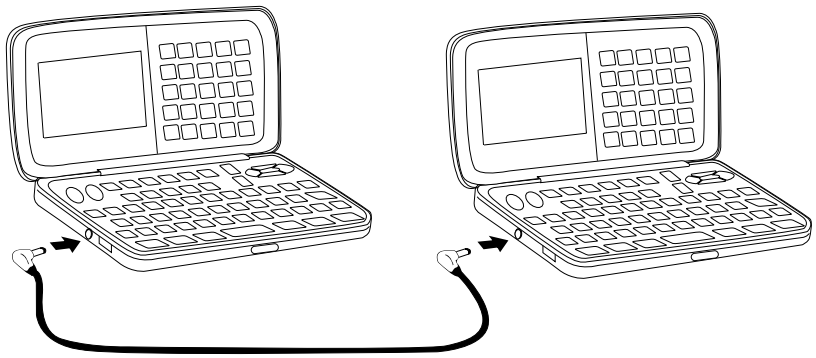
7. TO SAVE THE DATA TO OTHER MACHINE

SF-5600AR can transfer customers data to other SF-5600AR with memory protection only when replacing the LCD or the outer case.

How to transfer the data

* Before connecting the cable (SB-60 or SB-62), be sure to reset the slave machine to clear all data.

1) Turn off the power switch and connect the two units using the cable (SB-60 or SB-62) as shown in the drawing.



2) Turn on the power switch of each machine.

3) The slave machine must be set the date of Feb. 3rd, 1901 into the memory under the calculator mode.

Operation: [ON/CLEAR] [CAL] [1] [9] [0] [1] [DATE] [2] [DATE] [3] [DATE] [M+]

If you don't set the date, the "PASSWORD" isn't transferred to the slave machine.

4) Check the hardware parameters, and if the units have another condition, reset as follows.

To change the hardware parameters, press the [◁], [▷], [△] and [▽] cursol keys.

To set the hardware parameters, press the [SET] key.

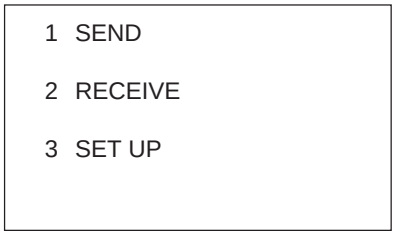
[TEL] [FUNCTION] [FUNCTION] [4] [3]

SET UP	
PARITY	NONE
BIT LENGTH	7
BPS	9600

5) Set up the slave machine.

1 While in the Calendar Display, Telephone Directory, Business Card Library, Memo Mode, or Schedule Keeper, press the [FUNCTION] key twice followed by [4] to select " DATA COMM", and the following menu appears.

TEL [FUNCTION] [FUNCTION] [4]



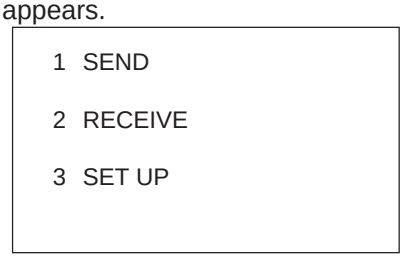
2 Press [2] to select "RECEIVE" and the following display appears to indicate that the slave machine is ready to receive data.

[2]

6) Set up the customer's machine.

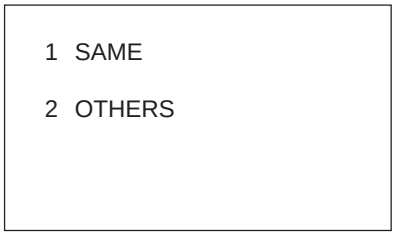
1 While the transmitting unit is in the Calendar Display, Telephone Directory, Business Card Library, Memo Mode, or Schedule Keeper, press the [FUNCTION] key twice followed by [4] to select "DATA COMM", and the following menu appears.

TEL [FUNCTION] [FUNCTION] [4]



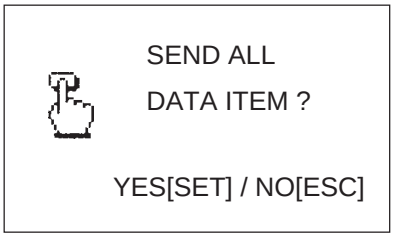
2 Press [1] to select "SEND" and the following menu appears.

[1]



3 Press [1] to select "SAME", then press [3] to select "ALL DATA". The following display appears to confirm whether you wish to proceed.

[1] [3]



4 Press the [SET] key to proceed with the data transmission, or press [ESC] if you wish to cancel.

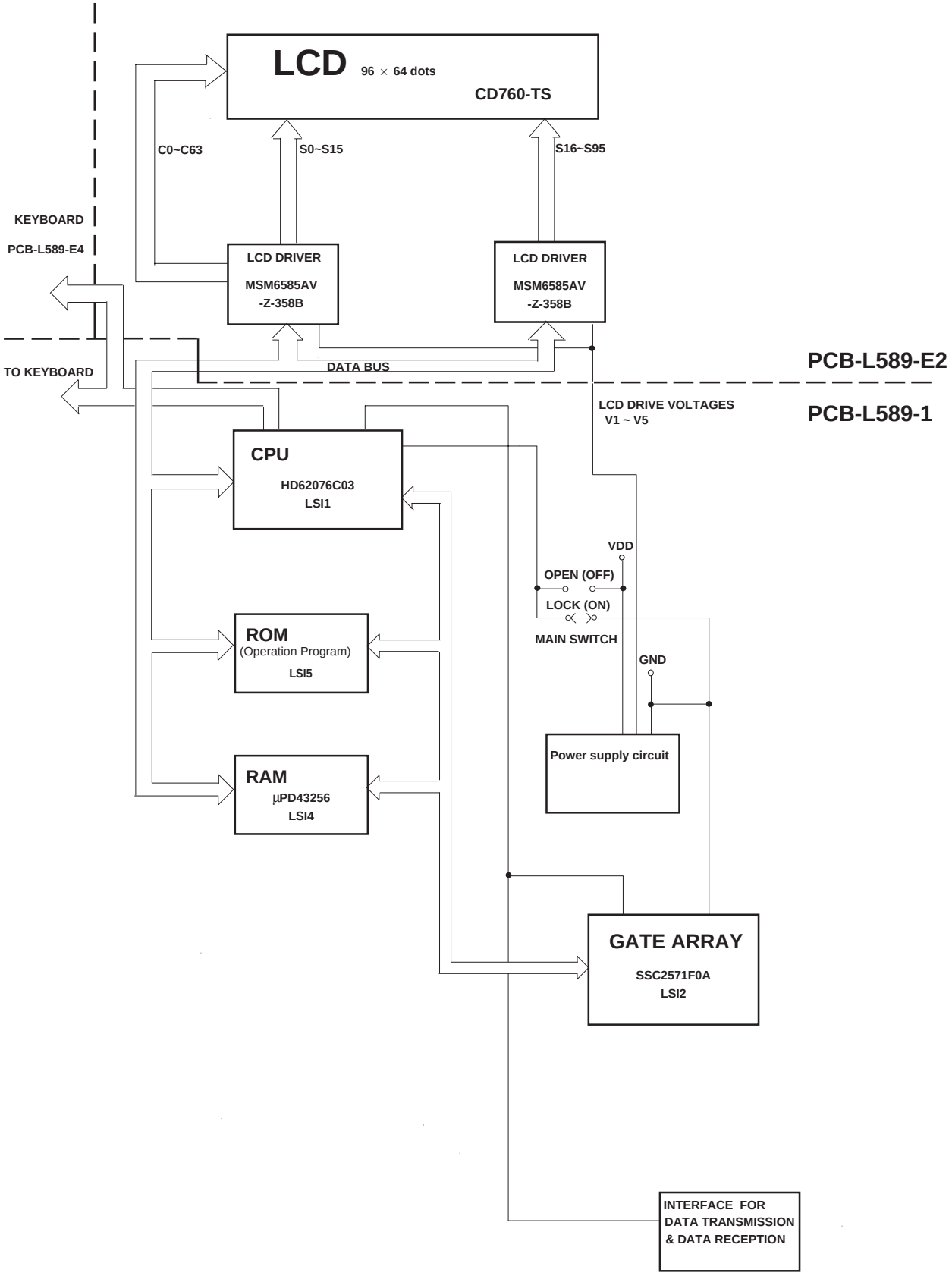
[SET]

Data are transmitted in the sequence of Telephone Directory data, Memo data, Reminder data, Schedule Keeper data and Calendar data.

* The following messages appear on the display of the receiving unit when a problem occurs during data communications. All data transferred up to display of the message is retained in memory, but data communication is terminated.
  If one of the following error messages appear, press the [TEL], [MEMO], [SCHEDULE], [HOME/WORLD], [REMINDER], [CAL], [CALENDAR] keys, to clear the error message. Then, take corrective action and try data communication again.

Message	Meaning	Action
TRANSMIT ERROR! STOPPED!	Error during data communications.	Cancel the data communications operation and try again.
DATA ERROR! CONSULT THE OWNER'S MANUAL!	Data corrupted by strong impact, electrostatic charge, etc.	See page 9 of the owner's manual.

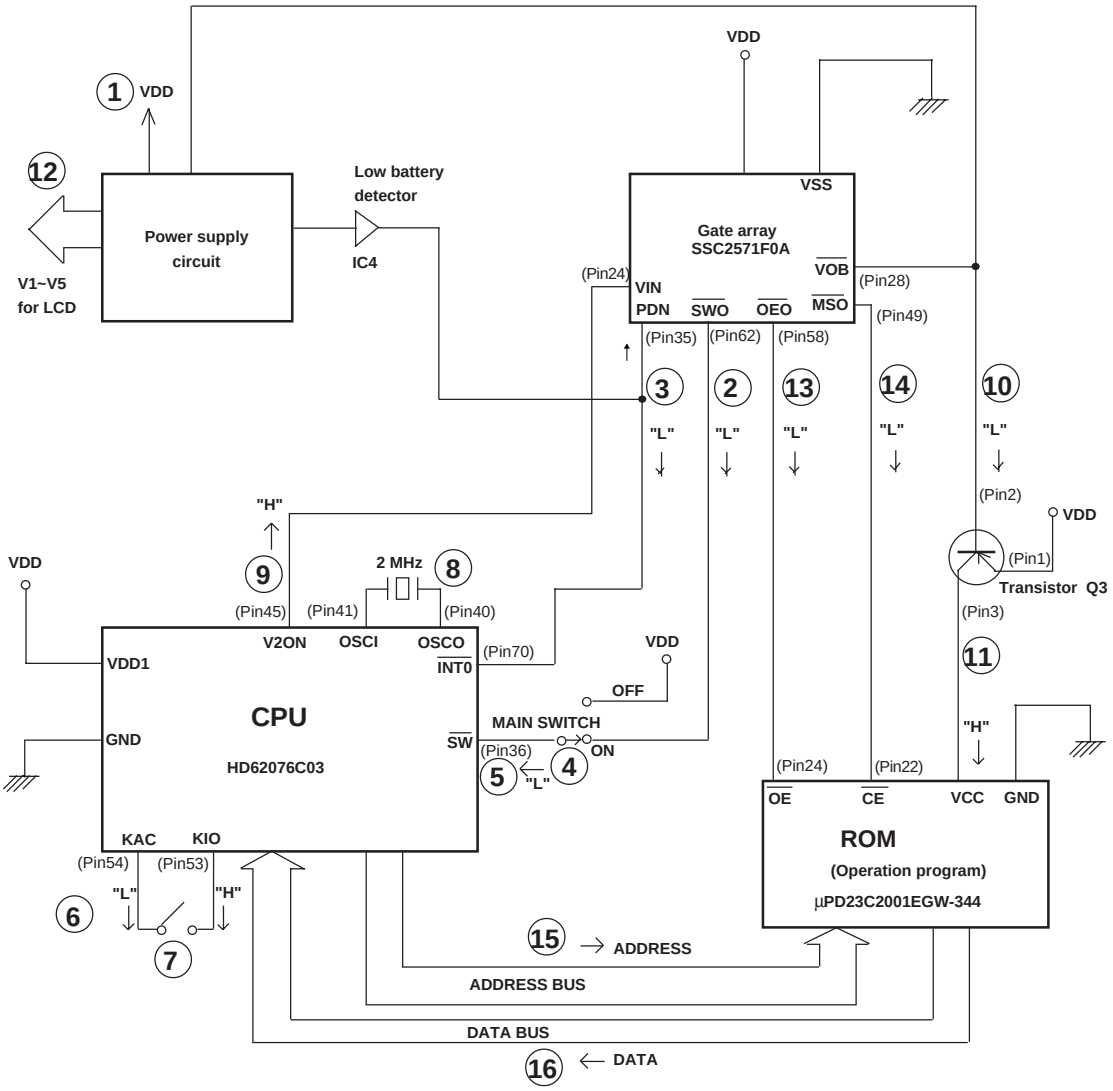
8. BLOCK DIAGRAM



9. CIRCUIT EXPLANATIONS

9-1. System chart

Generally, SF-5600AR is working with the following steps.



1. Supply 5V to VDD1 and VDD2.
2. Output "L" from $\overline{\text{SWO}}$ terminal.
3. Output "L" from IC4 and Q5 terminal.
4. Main switch ON.
5. Input "L" to $\overline{\text{SW}}$ terminal.
6. Input "L" from KAC terminal.
7. Push power on button switch.
8. CPU oscillation is generated.
9. Output "H" from V2ON terminal.
10. Output "L" from $\overline{\text{VOB}}$ terminal.
11. Apply VDD to ROM.
12. Output all LCD drive voltages.
13. Gate array sends ROM output enable signal to $\overline{\text{OE}}$ terminal.
14. Gate array sends ROM Chip enable signal to $\overline{\text{CE}}$ terminal.
15. CPU sends address to ROM.
16. CPU receives data from ROM.

9-2. Power supply circuit

1) Power supply circuit for CPU, GATE ARRAY and RAMs.

When the main batteries are set, the voltage (9V) supplies at the terminal VDD1 of CPU (LSI1), GATE ARRAY (LSI2) and RAM (LSI4).
When IC2 receives a voltage, the regulated voltage (4V) will be applied to the GND lines from the terminal OUT (Pin No.1).

2) Power supply circuit for ROM

When the GATE ARRAY (LSI2) controls the terminal VOB (Pin No.28) with "L" level, the transistor 2SA1411 (Q3) will be turned ON, then the voltage of the VDD lines will be applied the VCC lines.
The voltage of the ROM (LSI5) is supplied from the VCC lines.

3) Main switch

The CPU (LSI1) detects the informations of the Main switch by the terminal SW (Pin No.36) from the SWO signal of the GATE ARRAY (LSI2).

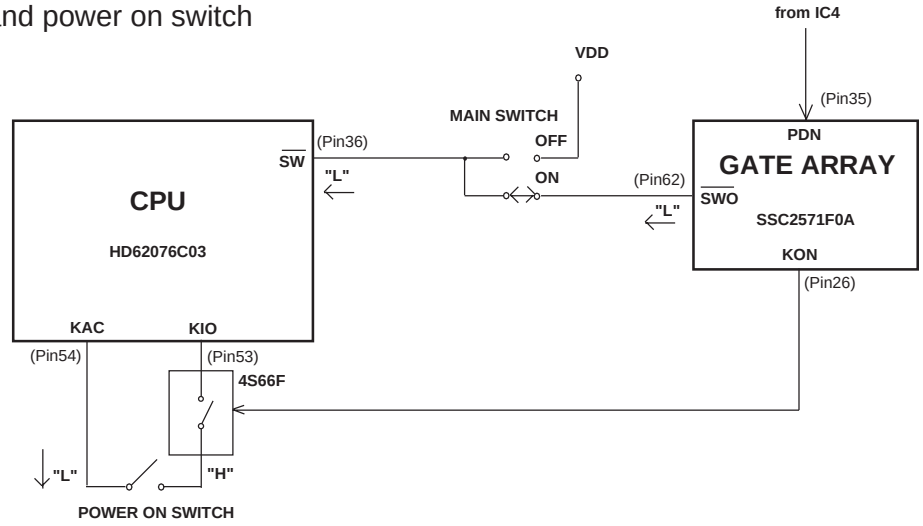
4) How to turn the display ON.

When pressing "ON" key under the ON side of the Main switch , the CPU (LSI1) generates the signal to turn the display ON at the terminal V2ON (Pin No.45).
This signal goes to the terminal VIN (Pin No.24) of the GATE ARRAY (LSI2), then the GATE ARRAY (LSI2) generates "L" level at the terminal VOB (Pin No.28). When the transistor 2SA1179 (Q2) receives "L" level, the transistor 2SC2812 (Q1) will be turned ON also. Then LCD drive voltage V1~V4 will be applied.

5) How to detect the voltage for the main batteries.

When the voltage of the VDD lines becomes +6.6V±0.18V, the terminal OUT (Pin No.1) of the detector RH5V60BA (IC4) becomes "L" level, then this signal goes to the terminal INTO (Pin No.70) of the CPU (LSI1) and the terminal PDN (Pin No.35) of the GATE ARRAY (LSI2).
The CPU detects the low battery condition, then the display turns OFF.

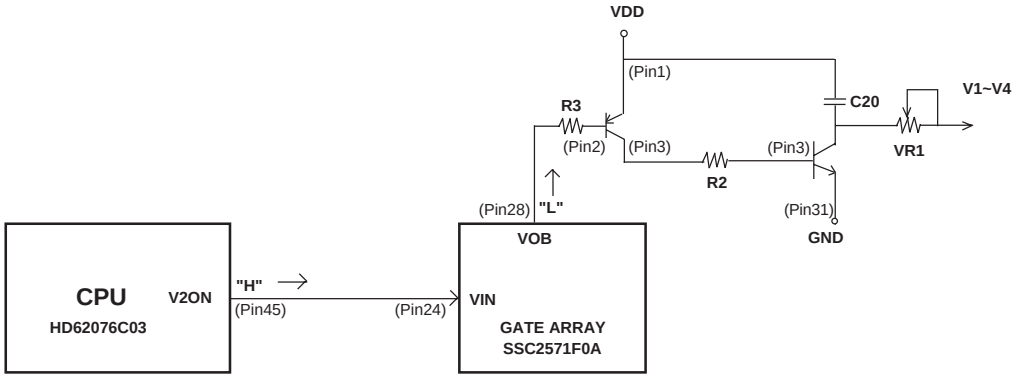
6) Main switch and power on switch



When the main switch is set to on position, $\overline{SW}$ terminal of CPU becomes "L", then CPU will send "L" signal to KAC terminal to enable the system power on. The KI0 terminal is "H" when VDD is applied to CPU. Therefore, when pressing the power on switch, CPU will generate a clock pulse (2 MHz) for start up the system.

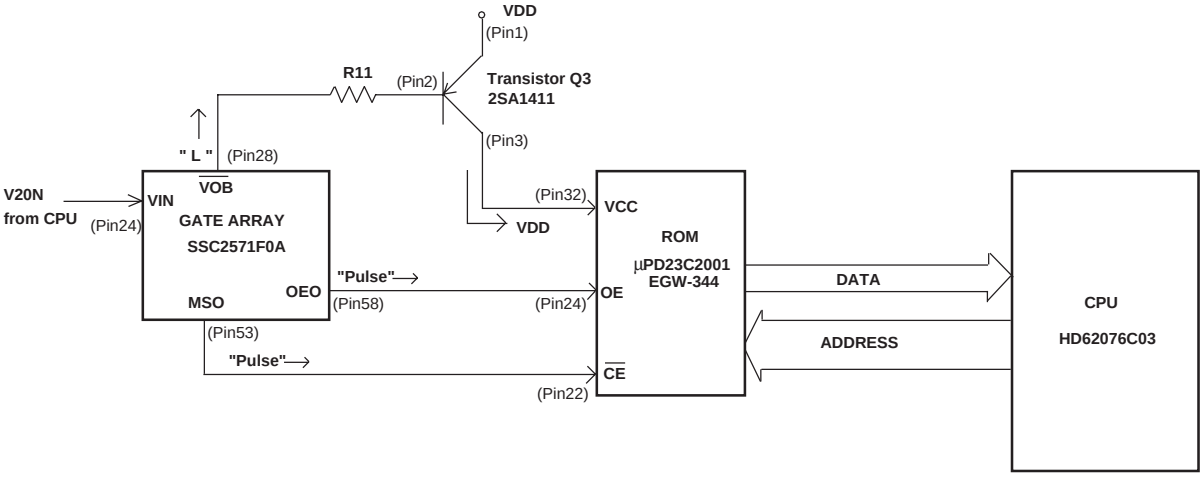
When the PDN terminal will be receiving "L" level, GATE ARRAY will send "L" signal from KON terminal for cutting the line of power on switch.

7) Power supply for LCD



When the system is start up, CPU will send "H" signal to VIN terminal of gate array from V2ON terminal. Then, gate array will send "L" signal from VOB terminal to turn ON the transistor Q2 and Q1 for LCD drive voltages.

8) ROM driving transistor



After gate array gets V20N signal from CPU, gate array sends "L" signal from $\overline{\text{VOB}}$ terminal to base terminal of transistor Q3. Then, the VDD is applied to ROM (operation program), CPU can read a ROM program data.

9-3. CPU pin description (HD62076C03)

Pin No.	Name	In/Out	Status of OFF	Status of ON	Description
1~14,16,17	A0~A15	Out	L	Pulse	Address Bus line
15,39, 100	VSS	In	GND	GND	GND terminal
24	WE	Out	H	Pulse	Write signal
25	OE	Out	H	Pulse	Read signal
26	FE	Out	H	Pulse	Chip select signal for Gate array
27	CS1	Out	H	H	Chip select signal
28	CS2	Out	H	H	Chip select signal
29	CS3	Out	H	Pulse	Chip select signal
30	E0	Out	L	Pulse	Chip enable signal (Not used)
31	E1	Out	L	H	Chip enable signal (Not used)
32	E2	Out	L	H	Chip enable signal (Not used)
33	E3	Out	L	H	Chip enable signal (Not used)
34	BCON	Out	H	H	BCN signal (Not used)
35	MDP2	Out	H	L	MDP signal (Not used)
36	SW	In	L	L	Switch signal (When switches are at ON position)
37	ONMK	In	H	H	Battery detection
38	TEST	In	L	L	TEST terminal (connect to GND)
40,41	OSC O/I	In	L	Pulse	Clock input
42	VDSC	In	L	H	Power input for Clock
43, 91	VDD1	In	H	H	VDD input terminal
44	VDD2	In	H	H	VDD input terminal
45	V2ON	Out	L	H	Power on output signal
46~53	KI7~KI0	In	H	H	Key input signal
54	KAC	Out	L	Pulse	Power on switch signal output
55~65,67	KC0~KC11	Out	H	Pulse	Key common signal output
66	GND	In	L	L	GND terminal
68	INT2	In	H	H	Interrupt signal from Gate array
69	INT1	In	L	H	Interrupt signal for transmission
70	INT0	In	H	H	Interrupt signal for Power down
71	BRK	In	H	H	VDD input terminal
72	P0	Out	H	H	Transmission data output
73	P1	In	L	H	Reception data input
74	P2	In	H	H	Card lock switch input (Not used)
75	P3	In	L	H	IC card detection signal input (Not used)
76	P4	Out	H	Pulse	Not used
77	P5	Out	H	Pulse	Not used
78	P6	In	H	H	Memory back-up battery detection input (Not used)
79	P7	In	H	H	Battery detection input (Not used)
80	H1	Out	H	H	Not used
81	WENL	In	L	L	GND terminal
82	H2	Out	H	H	Not used
83	L1	Out	L	H	Not used
84	L2	Out	L	L	Not used
85	DT	Out	H	Pulse	DT signal output
86	PRO	Out	L	H	LCD driver mode selection signal
87	FR	Out	L	Pulse	LCD driver synchronous signal
88	LP	Out	H	Pulse	LCD driver latch pulse signal
89	GC	Out	H	Pulse	GC signal output
90	DE	Out	H	Pulse	LCD driver data latch clock signal
92~99	IO7~IO0	In/Out	L	Pulse	Data bus line
18~23	RA14~19	Out	L	Pulse	Address line (Not used)

9-4. Gate array pin descriptions (SSC2571F0A)

Pin No.	Name	In/Out	Description
1	VSS1	In	GND terminal
2	OSO	Out	Clock out
3	OSI	In	Clock in
4	VL1	In	6V input
5~10	A0~3,A14,15	In	Address input
11	FE	In	Chip select signal from CPU
12	CS1	In	Chip select signal from CPU
13	CS2	In	Chip select signal from CPU
14	CS3	In	Chip select signal from CPU
15	OEI	In	Output enable signal from CPU
16	VSS(GND)	In	GND terminal
17	VH1(VCC)	In	9V input
18	TXI	In	Transmission data input from CPU
19	WEI	In	Write enable signal from CPU
20	GC	In	GC signal from CPU
21	IO0	In/Out	Data bus line
22	DT	In	DT signal input
23	IO1	In/Out	Data bus line
24	VIN	In	Power ON signal from CPU (V2ON)
25	IO2	In/Out	Data bus line
26	KON	Out	Switch control signal
27	IO3	In/Out	Data bus line
28	VOB	Out	Inverted signal for VIN
29	IO4	In/Out	Data bus line
30	INT	Out	Interrupt signal
31	VH2(VCC)	In	9V input
32	VL2(VLL)	In	6V input
33	VSS(GND)	In	GND terminal
34	BBC	Out	Not used
35	PDN	In	Power down detection input
36	IO5	In/Out	Data bus line
37	RLD	Out	Not used
38	RA15	Out	Address bus output
39	IO6	In/Out	Data bus line
40	RA16	Out	Inverted signal for VIN
41	IO7	In/Out	Data bus line
42	RA17	Out	Address bus output
43	RA18	Out	Address bus output
44	MS3	Out	Not used
45	RA19	Out	Not used
46	RA20	Out	Not used
47	R15	Out	Not used
48	VSS(GND)	In	GND terminal
49	VH3(VCC)	In	9V input
50	VDD1(VLL)	In	6V input
51	R16	Out	Not used
52	R17	Out	Not used
53	MSO	Out	Chip enable signal for ROM
54	MS4	Out	Chip select signal for RAM (Not used)
55	MS1	Out	Not used
56	MS5	Out	Chip select signal for RAM

Pin No.	Name	In/Out	Description
57	MS2	Out	Not used
58	OEO	Out	Output enable for ROM
59	BZ1	Out	Buzzer signal
60	OTP	In	Connected to GND
61	BZ2	Out	Buzzer signal
62	SWO	Out	Main switch control signal
63	VH4(VCC)	In	9V input
64	TXO	Out	Transmission data output terminal

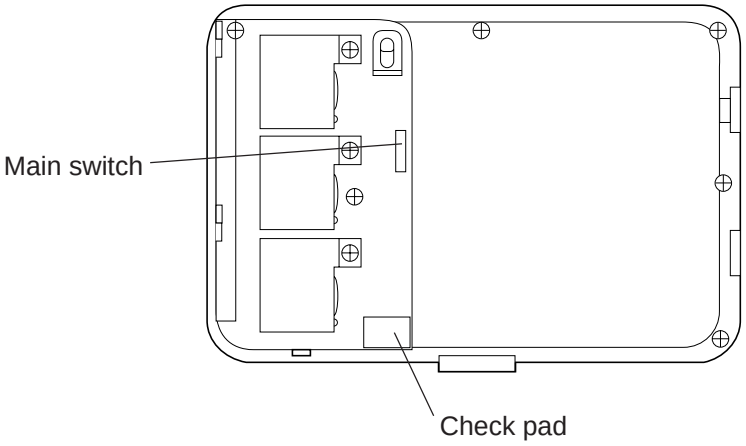
9-5. Operation program ROM pin descriptions

Pin No.	Name	In/Out	Status of OFF	Status of ON	Description
2~12,23, 25~30	A0~A17	In	L	Pulse	Address bus line (A0~A14, RA15~RA17)
13~15, 17~21	O0~O7	Out	L	Pulse	Data bus line (IO0~IO7)
16	GND	In	L	L	GND terminal
22	CE	In	H	Pulse	Chip enable signal from Gate array
24	OE	In	L	Pulse	Output enable signal from Gate array
31	PGM	In	L	Pulse	Address line (RA18)
1, 32	VPP, VCC	In	L	H	VDD terminal

9-6. RAM pin descriptions (μPD43256G)

Pin No.	Name	In/Out	Status of OFF	Status of ON	Description
1~10,21, 23~26	A0~A14	In	L	Pulse	Address bus line (A0~A14)
11~13, 15~19	IO0~IO7	Out	L	Pulse	Data bus line (IO0~IO7)
14	GND	In	L	L	GND terminal
20	CS	In	H	Pulse	Chip enable signal from Gate array
22	OE	In	L	Pulse	Output enable signal from Gate array
28	VCC	In	L	H	VDD terminal
27	WE	In	H	Pulse	Write enable signal from CPU

10. DIAGNOSTIC OPERATION




```
SELF TEST PROG.

  PRESS SET


    QUIT BY OFF

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```

1. Diagnostic mode

The diagnostic mode appears when main switch is turned on while there is a short in the checkpad. After this operation, the machine will beep and display "SELF-TEST".

```
MENU TOP SHEET
  1 : DISP CHECK
  2 : RAM TEST
  3 : MEMORY TEST
  4 : KEY / BUZZER
  5 : INTERFACE

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```

The menu appears after press SET key. Tests are conducted by selecting the mode from the list on screen. The each test can be selected by numeral keys.

DISPLAY TEST : Test the LCD disply
RAM TEST : Test the RAM chip
MEMORY TEST : Test the ROM/Clock
KEY/BUZZER : Test all keys and Buzzer
INTERFACE : Test the transmission

```
MENU DISPLAY
  1 : LCD ALIGNING
  2 : ALL DOTS ON
  3 : ALTERNATIVE
  4 : REVERSE
  5 : LCD FRAMING

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```

2. Display check

DISP CHNG key : Return to menu display

LCD ALIGNING: Lights on dot at corners
ALL DOTS ON : Lights on in all dots (black screen)
ALTERNATIVE : Checker display
REVERSE : Reverse checker display
LCD FRAMING : Lights on dot along the screen edge (frame)

3. RAM check

DISP CHNG key :Return to menu

```
MENU RAM                    #1
  1 : DATE WRITE
  2 : DATA READ
  3 : PAT. CHANGE
  4 :
  5 :

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```

DATA WRITE : Write the set pattern to the RAM area
DATA READ : Compare the pattern displayed after # with the write data of RAM and displays the results.
PAT. CHANGE : Change the test data pattern.

#1---Test data pattern(00,01,02...)
#2---Test data pattern(FF,FE,FD....)

1) RAM write

The machine will beep after a second. The menu will be appeared.

```
RAM WRITING                 #1

  NOW EXECUTING!



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```

It means RAM write is succeeded.

When there is no RAM to write a data, the following message will be displayed.

```
NO RAM
```

To release this message, press DISP CHNG key.

2) RAM read

Normal end display is;

```
RAM COMPARE                 #1

  COMPLETE!



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```

Error end display is;

```
RAM COMPARE                 #1

  DATA ERROR!
ADDRESS     CORR      RAM
  XXXX        XX        XX


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```

To release this message, press DISP CHNG key.

4. ROM/Clock check

```
MENU MEMORY
 1 : CHECK–SUM
 2 : SPECIFIC ADDR
 3 : TIME DISPLAY
 4 :
 5 :

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```

CHECK-SUM : Call up check sum and XOR values for connected ROM.
SPECIFIC ADDR : Call up check sum for certain address.
TIME DISPLAY : Bring up clock display. The present time, date and daily alarm can be set.

1) Check sum

```
CHECKSUM CALC

  TP      SZ       SUM      XOR
C0 O      256      0E0C      94



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```

2) Specific address

```
SPECIFIC ADDR

  TP      SZ       SUM      XOR
D0 O      256      XXXX      XX



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```

3) Time display

```
TIME DISPLAY

 1990-03-00

        10:10  00
XXXXXXXXXXXXXXX

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```

Input can be made in the line which shows "x" using the numeric keys. Entry of 12 or more digits sets the time and date. Entry of 4 or 6 digits sets the daily alarm. The [ON] key clears current entries.

5. Key/Buzzer check

```
MENU KEY / BZR
 1 : RANDOM
 2 : COMPULSORY
 3 : BEEP
 4 : ALARM NOTE 1
 5 : ALARM NOTE 2

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```

RANDOM :
The 'key code' will be displayed. The 'key code' is numbered incrementally from left to right with the [DATE] key as "00", and [HOME/WORLD] key as "34" etc. Accordingly, the left cursor key is "40". To release this test, press [SEARCH] key.

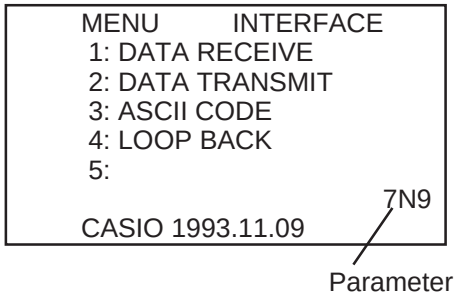
COMPULSORY :
Limits the mode mentioned above so that the keys must be pressed in order according to the key code. If an error is made a buzzer sounds for about 1 second. (A correct entry results in a beep tone)

BEEP : Key input sound every 1 second
ALARM NOTE 1 : Sound alarm 1
ALARM NOTE 2 : Sound alarm 2

In either mode a press of the SEARCH key will return the screen to the menu mode.

Sound can be stopped by pressing the any key.
While an alarm is sounding the screen display is as shown at left. If an irregularity is found in voltage of battery while the alarm is sounding, the alarm will stop. After 256 seconds, the alarm will stop automatically.

6. Interface check



The three charactors that appear on the right side at display represent the parameter. In the case of the example display, it indicates 7 BIT, NON PARITY, 9600 BPS. The operation continues until stopped by pressing the ESC key and then pressing the ON key for all modes.

DISP CHNG key : Return to menu mode

1 key : Transmission mode. The data of transmission is "H" and it is sent out by the data of H34 and H38 by the Xon/Xoff control.

2 key : Reception mode. Make sure to set the parameter to match that of the transitting side. The data received appears on the display.

3 key : Output the following ASCII code by Xon/Xoff control.
!"#*+,-/0123456789:
ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
A line end code is added with each line.

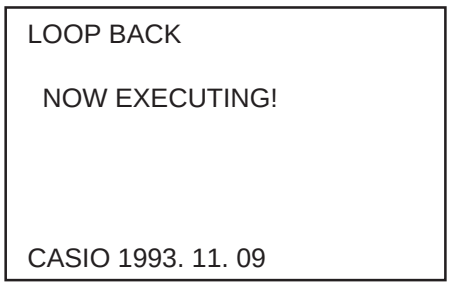
4 key : Loop back test. Short the Tx and Rx terminals for this test. Transmit and check from H20 to H7E. When complete, the message 'CHECK COMPLETE' is displayed.

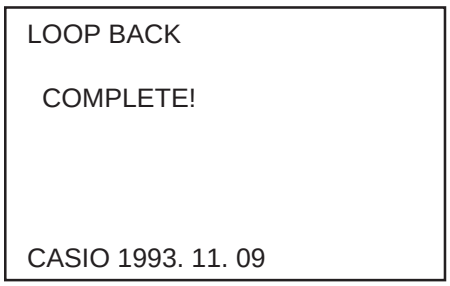
6 key : Switch the data length 7 bit(7) or 8 bit(8)

7 key : Switch the parity bit : NON(N)—EVEN(E) —NON(N) —ODD(O)

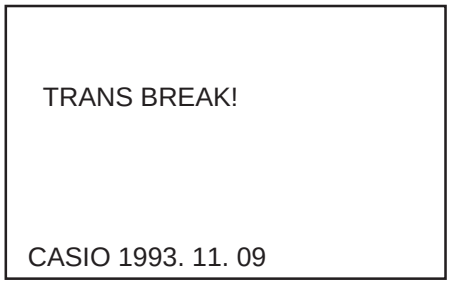
8 key : Switch the transmission speed : 9600(9)—4800(4)—2400(2)—1200(1)

NOTE : As diagnostic program area does not have all ASCII code, to display a reception data, some charactor will be changed to other charactor. For example, a chapital letter will be changed to small letter.

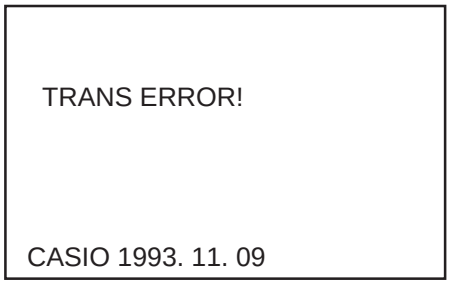




Break display (Broken transmission)



Error display

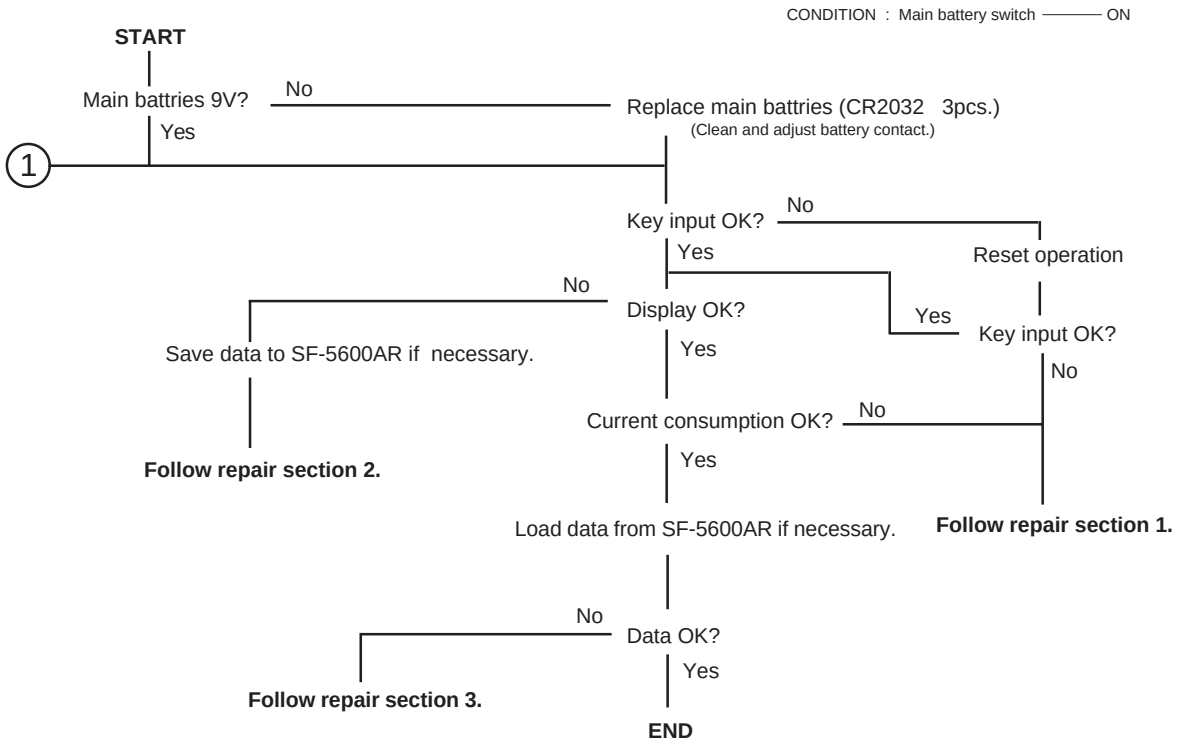


7. Others

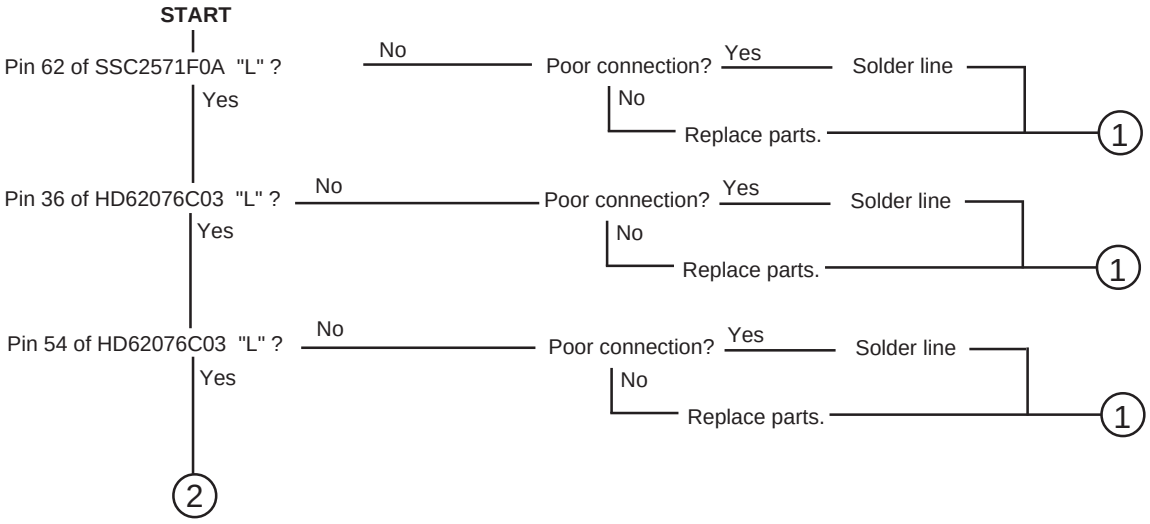
1) When power is off after presetting a alarm time, automatically power is on at a alarm time. However, the display is not reserved in this case.
2) When executing memory sum check, before execute the RAM write check.
3) To release diagnostic mode, press RESET button.
4) The display contrast can be changed by the contrast volume.

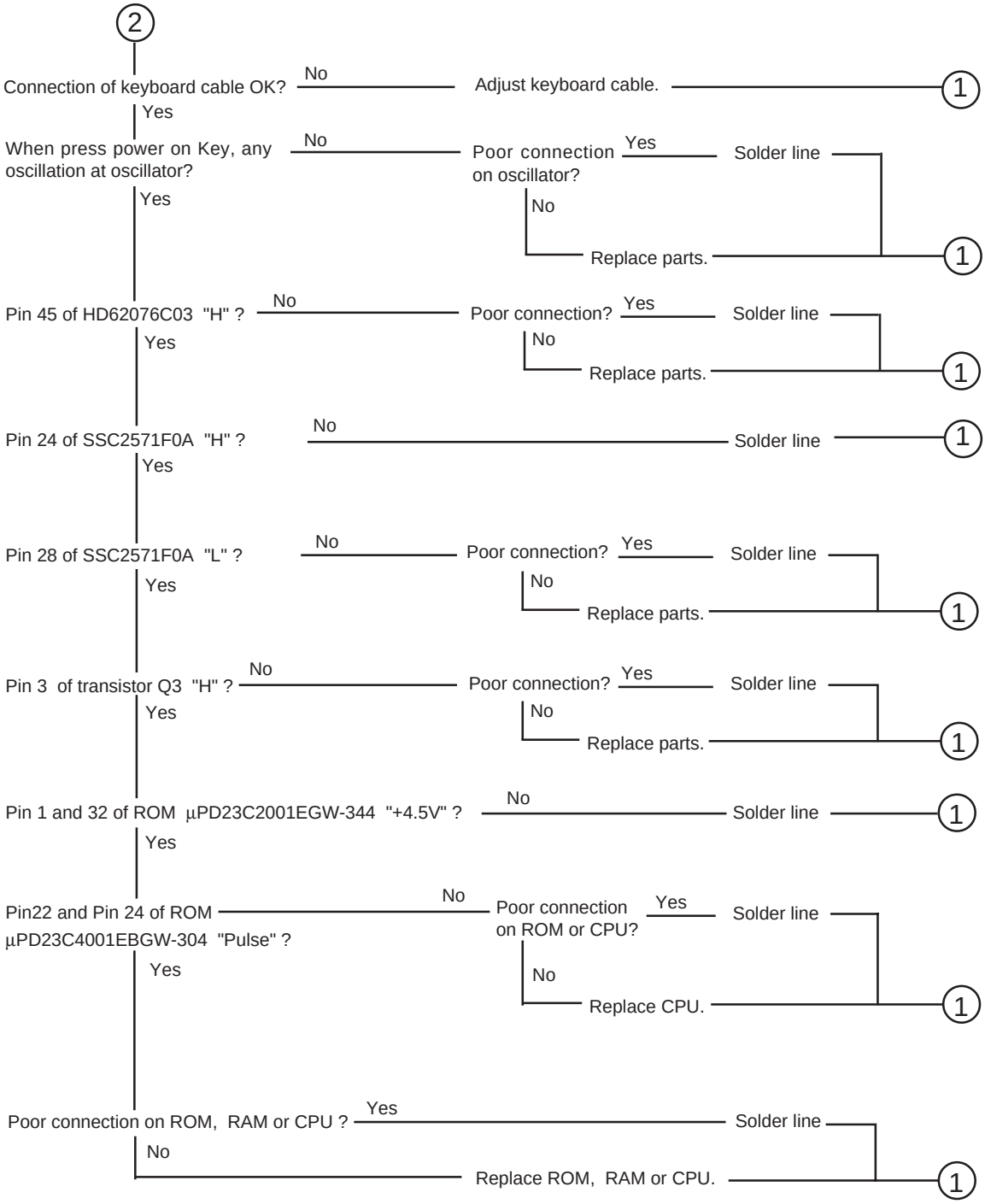
11. TROUBLESHOOTING

Generally, check the machine with the followning steps for repair.

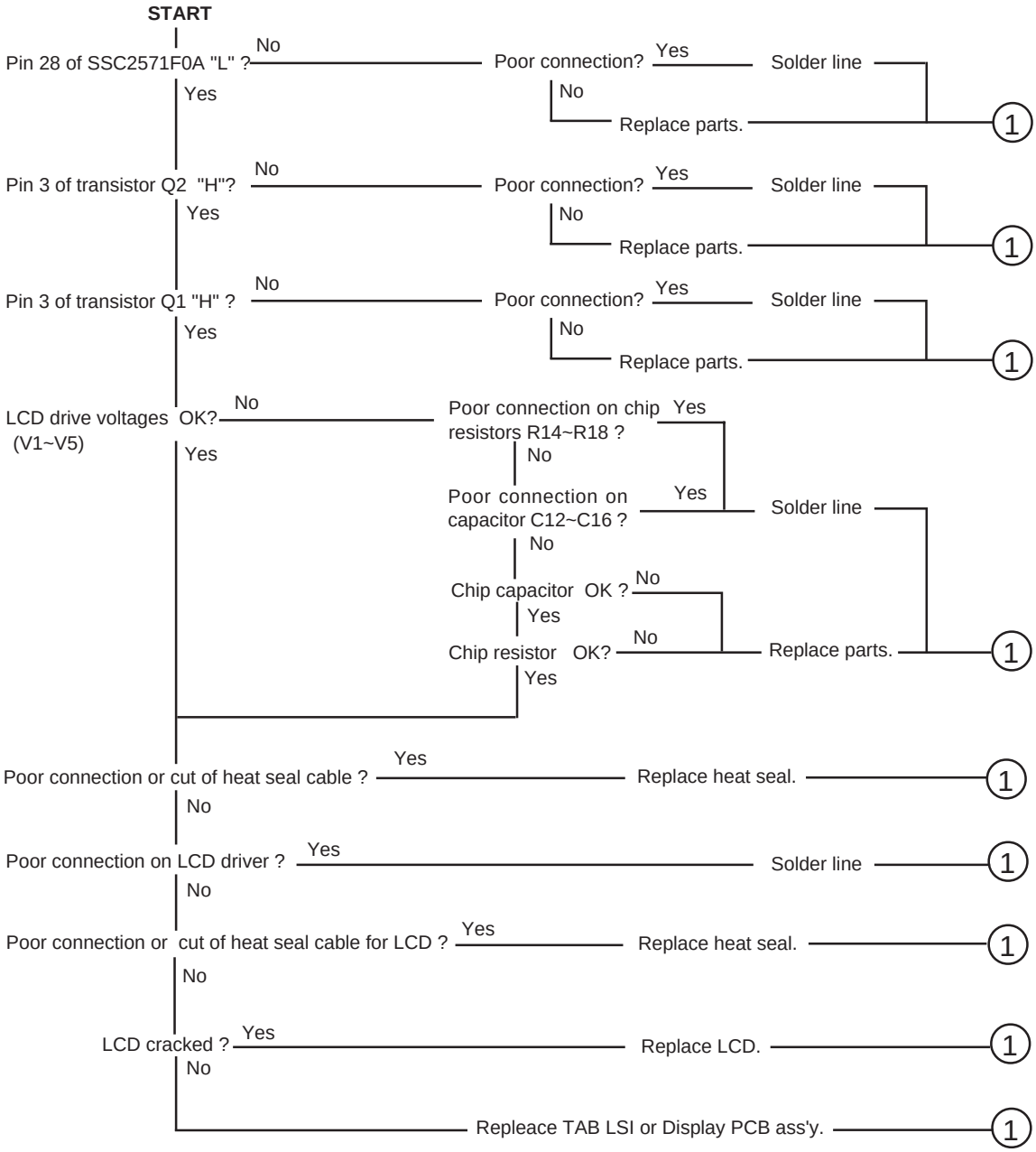


Repair section 1 : For no key input problem

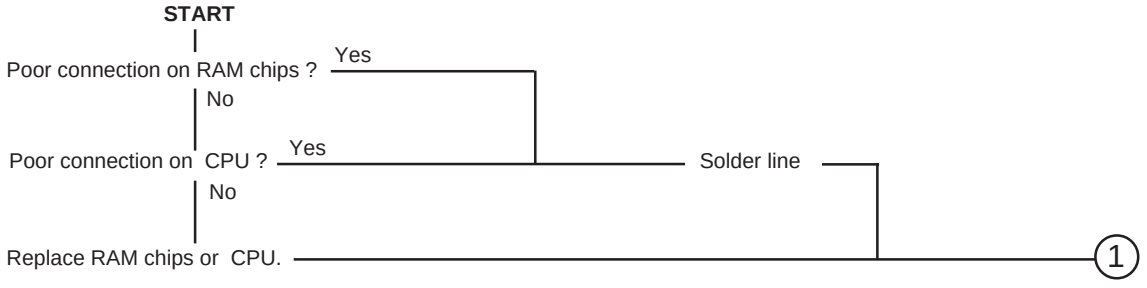



2
Connection of keyboard cable OK?
No
Adjust keyboard cable.
1
Yes
When press power on Key, any oscillation at oscillator?
No
Poor connection on oscillator?
Yes
Solder line
No
Replace parts.
1
Yes
Pin 45 of HD62076C03 "H" ?
No
Poor connection?
Yes
Solder line
No
Replace parts.
1
Yes
Pin 24 of SSC2571F0A "H" ?
No
Solder line
1
Yes
Pin 28 of SSC2571F0A "L" ?
No
Poor connection?
Yes
Solder line
No
Replace parts.
1
Yes
Pin 3 of transistor Q3 "H" ?
No
Poor connection?
Yes
Solder line
No
Replace parts.
1
Yes
Pin 1 and 32 of ROM µPD23C2001EGW-344 "+4.5V" ?
No
Solder line
1
Yes
Pin22 and Pin 24 of ROM µPD23C4001EBGW-304 "Pulse" ?
No
Poor connection on ROM or CPU?
Yes
Solder line
No
Replace CPU.
1
Yes
Poor connection on ROM, RAM or CPU ?
Yes
Solder line
No
Replace ROM, RAM or CPU.
1

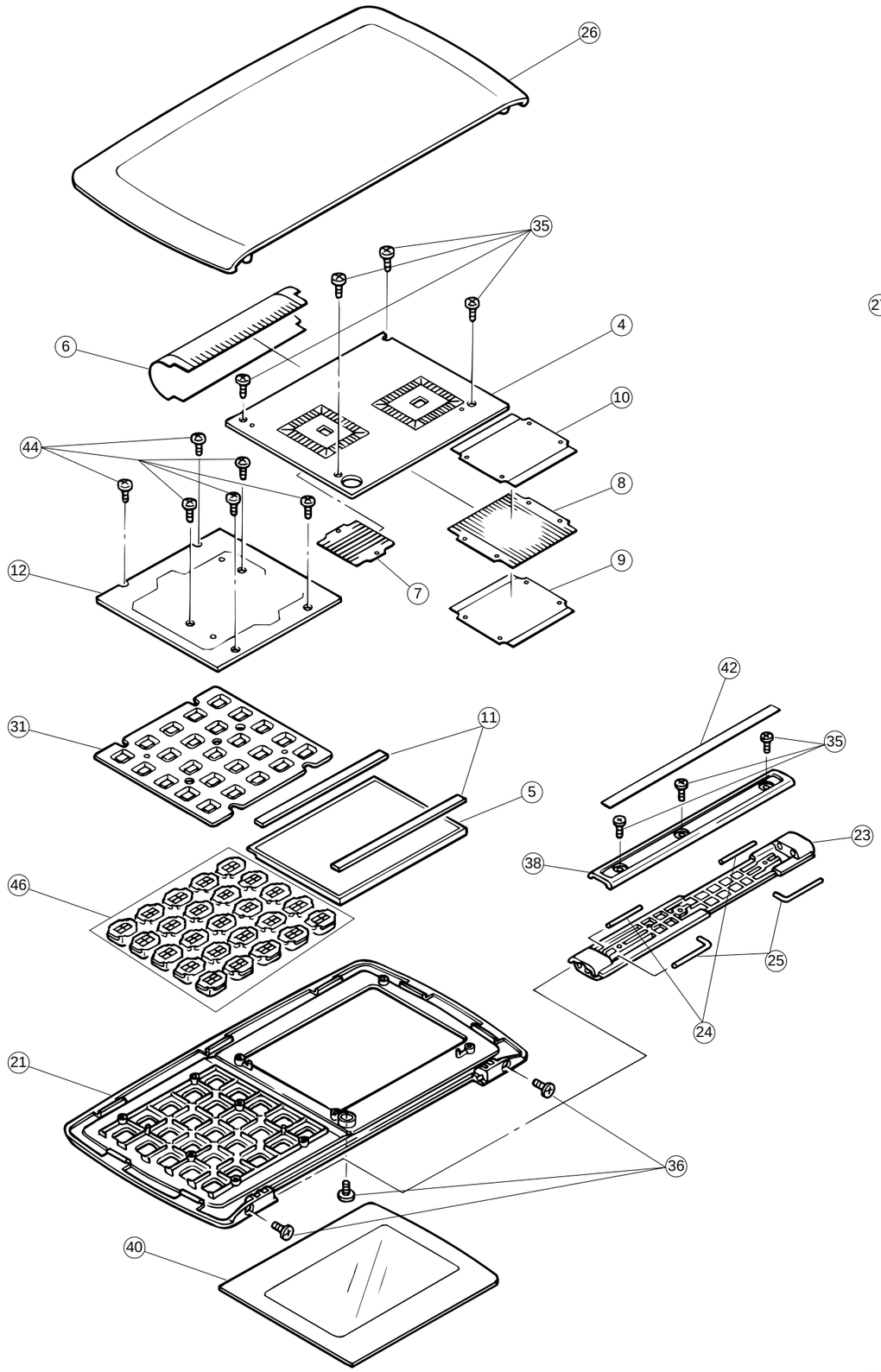
Repair section 2 : For no display or wrong display problem

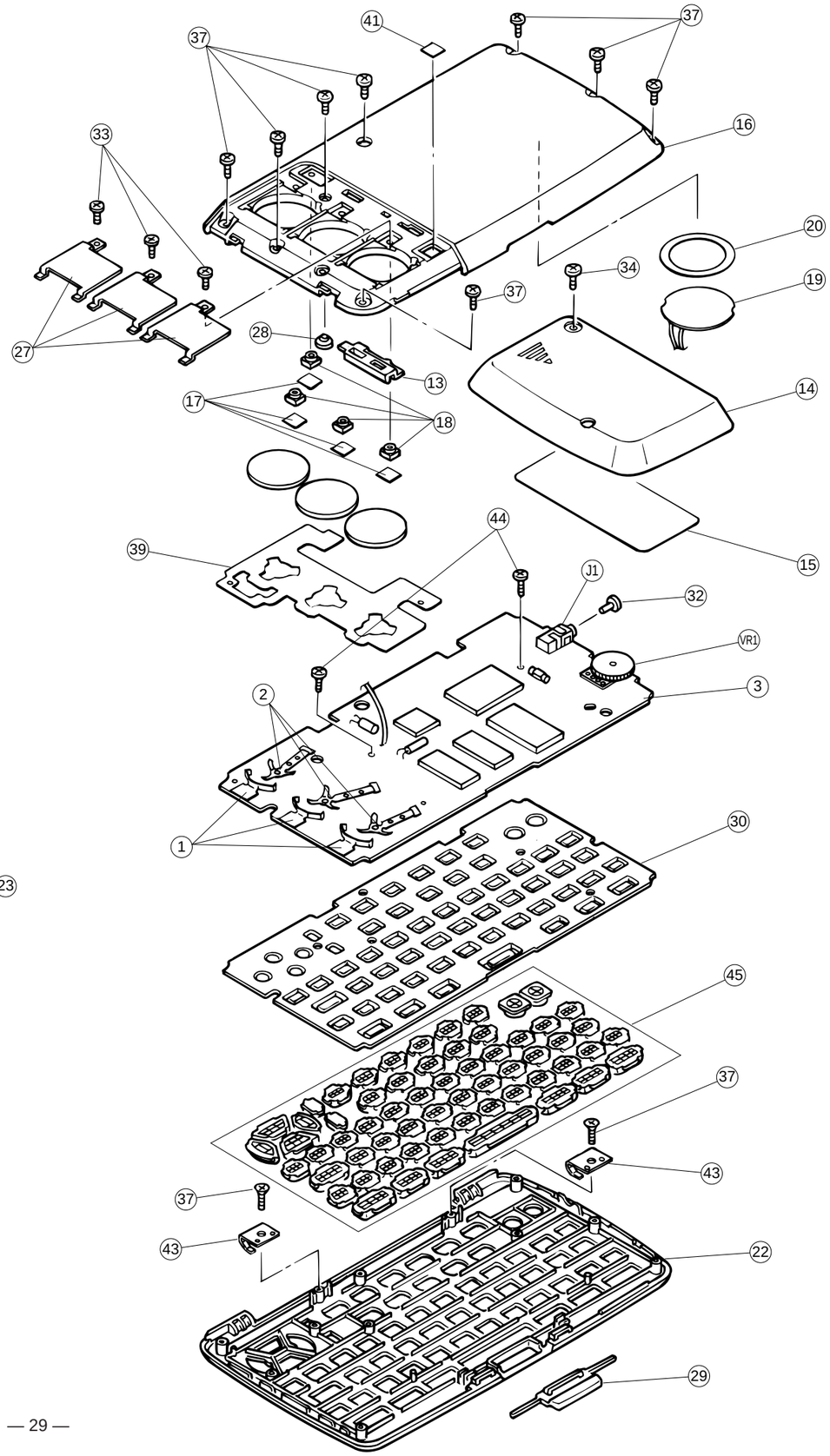


Repair section 3 : For memory problem



12. ASSEMBLY VIEW





13. PARTS LIST (SF-5600AR)

N	Item	Code No.	Parts Name	Specification	Q	M	FOB Japan N.R.Yen Unit Price	R
		1. MAIN BOARD						
N	LSI1	2011 3843	LSI (CPU)	HD62076C03	1	1	720	A
N	LSI2	2011 7350	LSI (G.A.)	SSC2571F0A	1	1	460	A
	LSI4	2011 2849	LSI (RAM)	µPD43256AGU-1012LL	1	1	600	A
N	LSI5	2011 7343	LSI (ROM)	µPD23C2001EGW344	1	1	490	A
N	IC1	2105 3031	C MOS IC	XC62DN2502PR	1	5	63	B
	IC2	3122 0476	Regulater	S-80250AG-GB	1	1	100	B
N	IC3	2105 3493	C MOS IC	S-81220PG-PS	1	10	47	B
	IC4	2105 2247	C MOS IC	RH5VA60BA-T1	1	10	65	B
N	IC4	2105 3794	C MOS IC	S-80766AL	1	5	70	B
	IC6	2105 1141	L-MOS IC	TC4S66F-TE85R	1	5	39	B
	Q1	2221 0378	Chip transistor	2SC2812-L5,L6-TB	1	20	12	B
	Q2	2200 4417	Chip transistor	2SA1179M5,M6-TB	1	20	15	B
	Q3	2250 0413	Chip transistor	2SA1411-T1B (M16)	1	20	24	B
	Q4	2259 0959	Chip digital transistor	DTC114YKT-146	1	20	12	B
	Q5	2200 4417	Chip transistor	2SA1179M5,M6-TB	1	20	15	B
	D1	2390 0847	Chip diode	MA718-(TX)	1	5	48	B
	D2	2390 0469	Chip diode	MA157A-(TX)	1	10	19	B
	D3	2390 0364	Schottky diode	MA713-TX	1	10	33	B
	X1	2590 0777	Ceramic oscillator	CSA2.01MGCM001-TC	1	5	98	B
	X2	7110 0642	Crystal oscillator	DT-26S	1	10	57	B
	C1	2802 9742	Electrolytic capacitor	16MS510-T3	1	10	13	B
	C4	2845 2289	Chip capacitor	MCH215C471KK	1	20	3	C
N	C5	2845 1673	Chip capacitor	MCH215A221JK	1	20	4	C
	C6,7	2845 2499	Chip capacitor	MCH215A300JK	2	20	3	C
N	C8,9	6411 8550	Chip capacitor	CP016F602T3	2	20	5	C
	C10~16	2845 1540	Chip capacitor	MCH212F104ZK	7	20	4	C
N	C20	2845 3570	Chip capacitor	MCH312F474ZK	1	20	13	C
	CB1~4,6,7	2845 1540	Chip capacitor	MCH212F104ZK	6	20	4	C
	R1,2	2795 1309	Chip resistor	MCR10EZHJ684	2	10	9	C
	R3,22	2795 0532	Chip resistor	MCR10EZHJ105	2	20	3	C
	R6,7	2792 0217	Chip resistor	MCR10EZHJ101	2	20	3	C
	R10	2792 0462	Chip resistor	MCR10EZHJ473	1	20	3	C
	R11	2792 0977	Chip resistor	MCR10EZHJ154	1	10	9	C
	R12	2792 1191	Chip resistor	MCR10EZHJ182	1	10	9	C
	R13	2792 0470	Chip resistor	MCR10EZHJ102	1	20	3	C
N	R14~18,23	2730 0591	Chip resistor	MCR10EZHG332	6	20	2	C
	R19	2792 0209	Chip resistor	MCR10EZHJ104	1	20	3	C
	R26,28,29	2795 0056	Chip resistor	MCR10EZHJ000	3	20	3	C
N	VR1	6411 8480	Volume	CF10013A008	1	5	90	C
	J1	3501 6405	Miniature jack	HSJ1169-012010	1	5	56	X
N	1	6411 8490	Battery spring (+)	EF01DB21109	3	20	12	X
	2	6409 6310	Battery spring (–)	EF02DB10100	3	20	16	X
N	3	6410 8520	CPU board ass'y (Consists of above parts)	DB21XX3100R*1	1	1	3,800	B

Notes: N – New parts
M – Minimum order/supply quantity
R – Rank
Q – Quantity used per unit

R – A : Essential
B : Stock recommended
C : Others
X : No stock recommended

N	Item	Code No.	Parts Name	Specification	Q	M	FOB Japan N.R.Yen Unit Price	R
		2. DISPLAY BOARD						
	LSI6,7	2011 1974	TAB LSI	MSM6385AV-Z-358B	2	1	370	A
N	4	6411 8440	D/D board ass'y (Consists of above parts)	DB21XX3F00M*1	1	1	940	B
		3. COMPONENT						
N	5	3335 4753	LCD	CD781-TS	1	1	610	A
N	6	6411 6340	Heat seal	FX20P320003	1	1	200	A
N	7	6512 1280	Heat seal	FX200P80074	1	10	49	B
N	8	6512 1230	Heat seal	FX200P60014	1	1	120	A
N	9	6512 1240	Protection tape	HGFC0007409	1	20	22	B
N	10	6411 8470	Protection tape	HGJ00003706	1	20	22	B
N	11	6411 8460	Cushion	FH100027205	2	20	18	C
N	12	6411 8450	Keyboard PCB	DADB21XX304	1	5	65	X
	13	6408 5920	Switch knob ass'y	DB2AXX4A00M	1	1	30	C
N	14	6411 8420	Battery cover	FADDB211006	1	20	27	X
N	15	6411 8430	Battery cover label	HGFC0009908	1	20	15	X
N	16	6411 8410	Lower case (KB)	FABDB211000	1	5	95	X
	17	6510 4440	Insulation seal	HGFC0001206	4	1	6	X
	18	6512 1080	Nut	MD100000602	4	1	15	X
	19	3122 2380	Buzzer	EFB-S55C41A8	1	1	36	X
	20	6510 4500	Buzzer tape	HGFC0000501	1	1	17	X
N	21	6411 8380	Upper case (DIS)	FAADB212000	1	5	68	X
N	22	6411 8390	Upper case (KB)	FAADB211003	1	1	250	X
N	23	6411 8400	Hinge A	FC0DB061009	1	20	21	X
N	24	6512 1210	Pin	FC002870000	2	20	9	X
N	25	6512 1220	Pin (L)	FC002870018	2	20	16	X
N	26	6411 8240	Lower case (DIS)	FABDB212006	1	5	95	X
	27	6409 6120	Battery holder	ECDB1011108	3	1	26	X
	28	6511 8400	Key contact rubber C	LADB0220105	1	1	10	C
N	29	6411 8250	Knob	FB3DB211007	1	20	9	X
N	30	6411 8260	Key contact rubber (61)	LADB2110005	1	1	200	C
N	31	6411 8270	Key contact rubber (25)	LADB2120001	1	5	83	C
	32	6511 7160	RB insert	LC120000102	1	1	17	C
	33	6510 4310	Decoration screw	MAA80006311	3	1	3	B
	34	6510 4350	Decoration screw	MAA80006302	1	1	2	B
N	35	6512 1000	Screw	MABA0004207	7	20	3	C
	36	6510 5260	Screw	MAB10032301	3	1	3	C
N	37	6406 8750	Screw	MAB20070302	10	20	10	C
N	38	6411 8340	Hinge B	FC0DB062005	1	20	18	X
N	39	6411 8350	Battery insulation	EL4F0002103	1	20	24	X
N	40	6411 8360	Display plate	EL5F0008103	1	1	170	B
N	41	6512 0870	Mask tape	HGFC0006909	1	20	4	X
N	42	6512 0860	Hinge tape	HGFC0007000	1	20	22	C
N	43	6512 0730	Hinge stopper	EF15DB06102	2	10	27	X
N	44	6411 8370	Screw	MABA0006307	8	20	3	X
N	45	6411 8290	Alphabet key set	KGDB2110009	1	1	120	X
N	46	6411 8300	Numeric key set	KCDB2120008	1	1	120	X

Notes: N – New parts
M – Minimum order/supply quantity
R – Rank
Q – Quantity used per unit

R – A : Essential
B : Stock recommended
C : Others
X : No stock recommended

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